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(54) Signal processing techniques based upon optical devices

(57) A signal processing system processes an input signal in real time. The system includes a light valve array for selectively attenuating light incident thereupon in response to electronic control signals, a light source for providing illumination, a light-sensitive array for producing electronic output signals representing a processed version of the input signal in response to light incident thereupon, and control circuitry for generating and applying electronic control signals to the light valve array in response to the input signal. The electronic control signals are generated from the input signal and are adapted for implementing an arbitrarily-selected signal processing operation. The light valve array is situated between the light source and the light-sensitive array, such that the light source is selectively attenuated by the light valve array, and such that the selectively attenuated light is incident upon the light-sensitive array.

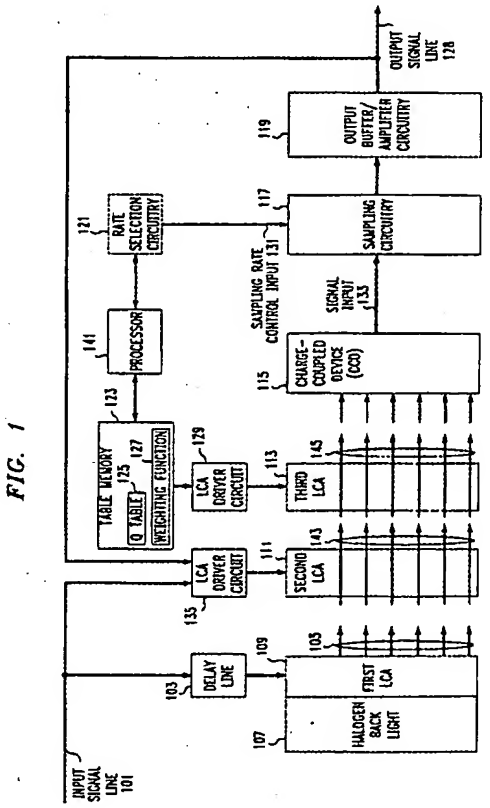

FIG. 1

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Description

1. Background Of the Invention

The invention relates to optical devices for signal processing.

2. Description of Prior Art

In the past, linear signal processing operations have been performed by analog systems which utilize various configurations of active light sources, such as light emitting diodes (LEDs), in combination with area-array, charge-coupled devices (CCDs). These systems have also been used to implement electro-optical processors capable of performing complex mathematical operations. Such operations are often performed for the purpose of compressing and/or expanding data signals representing voice and video information, while maintaining the temporal relationship of the data signals. However, analog systems place inherent limitations on the maximum amount of data resolution that may be achieved. Furthermore, digital systems provide data manipulation capabilities that are unavailable or impractical to implement in the relatively harsh operational environment of the analog domain. The digital system provides more stable and predictable data manipulation. What is needed is a digital optical signal processing system which offers enhanced levels of resolution and flexibility relative to existing analog systems.

Summary of the Invention

A signal processing system processes an input signal in real time. The system is characterized by a light valve array for selectively attenuating light incident thereupon in response to electronic control signals, a light source for providing illumination, a light-sensitive array for producing electronic output signals representing a processed version of the input signal in response to light incident thereupon, and control circuitry for generating and applying electronic control signals to the light valve array in response to the input signal. The electronic control signals are generated from the input signal and are adapted for implementing an arbitrarily-selected signal processing operation. The light valve array is situated between the light source and the light-sensitive array, such that the light source is selectively attenuated by the light valve array, and such that the selectively attenuated light is incident upon the light-sensitive array.

Brief Description of the Drawings

FIG. 1 is a hardware block diagram setting forth a first embodiment of the optical signal processing system disclosed herein;

FIG. 2 is a hardware block diagram setting forth a second embodiment of the optical signal processing system disclosed herein;

FIG. 3 is a graphical representation of an illustrative image to be processed by the optical signal processing system of FIG. 2; and

FIG. 4 is a combined hardware and data structure diagram setting forth a third embodiment of the signal processing system disclosed herein for implementing JPEG video compression.

Detailed Description of the Preferred Embodiments

FIG. 1 is a hardware block diagram setting forth a first embodiment of the optical signal processing system disclosed herein. The optical signal processing system of FIG. 1 processes signals in real time using a first light valve device (first LCA 109), a second light valve device (second LCA 111), a third light valve device (third LCA 113), a fixed-value light source (halogen back light 107), and a charge-coupled device (CCD) 115.

The first LCA 109 is positioned between the halogen back light 107 and the second LCA 111. The second LCA 111 is positioned between the first LCA 109 and the third LCA 113. The third LCA 113 is positioned between the second LCA 111 and the CCD 115. The positioning of first, second, and third LCAs 109, 111, 113 with respect to halogen back light 107 and CCD 115 is implemented so as to enable the LCAs to selectively control the amount of light from the halogen back light which is incident upon the CCD.

The first LCA 109 is driven by the output of a delay line 103, the second LCA 111 is driven by LCA driver circuit 135, and the third LCA is driven by LCA driver circuit 129. Conventional devices may be employed to implement LCA driver circuits 129 and 135. Delay line 103 is of conventional design and may consist, for example, of a conventional memory buffer device. Third LCA driver circuit 129 is coupled to a table memory 123 which stores a Q table 125 of quantization coefficients, as well as a weighting function 127. A processor 141 accesses, controls, and indexes table memory 123. Processor 141 may be a microprocessor of conventional design, and table memory 123 may consist of any desired combination of conventional random-access memory (RAM) and/or read-only memory (ROM).

CCD 115 provides an output signal on signal line 133 which is coupled to sampling circuitry 117. Sampling circuitry 117 is digital sampling circuitry of conventional design which periodically samples the output of CCD 115. This sampling circuitry 117 includes a sampling rate control input 131 for determining the sampling rate of sampling circuitry 117. Rate selection circuitry 121 for determining and selecting a desired sampling rate is coupled to sampling rate control input 131. This rate selection circuitry 121 is controlled by processor 141. Although rate selection circuitry 121 and processor 141 are shown as separate elements in FIG. 1, it is possible to combine these elements, using processor 141 to per-

form the functions of rate selection circuitry 121. In this manner, the functions of the rate selection circuitry 121 block may be absorbed into the processor 141 block. The output of sampling circuitry 117 is coupled to output buffer/amplifier circuitry 119, which includes conventional video buffers and amplifiers.

The output signal produced by output buffer/amplifier circuitry 119 is coupled to LCA driver circuit 135. Therefore, the output of LCA driver circuit 135 used to drive second LCA 111 is a function of the input signal on input signal line 101, as well as the output signal on output signal line 128. The output of LCA driver circuit 129 used to drive LCA 113 is a function of the weighting function 127 and the Q table 125 stored in table memory 123. The output of delay line 103 used to drive first LCA 109 is a function of the input on input signal line 101.

The system of FIG. 1 operates as follows. Halogen back light 107 illuminates first LCA 109. A delayed version of the input signal on input signal line 101 is applied to the first LCA 109, affecting the degree to which various portions of LCA 109 attenuate the illumination from halogen back light 107. The light rays originating at halogen back light 107 traverse first LCA 109 and are selectively attenuated, forming a first set of rays 105. The first set of rays 105, incident upon second LCA 111, represent an optical version of the original input signal on signal line 101.

The second LCA 111 is driven with a combination of the original input signal on signal line 101 and the output signal on output signal line 128. First set of rays 105 traverse the second LCA 111 and are selectively attenuated, forming a second set of rays 143. The second set of rays 143 are incident upon third LCA 113, which is driven by a signal representing a weighting function 127. The particular weighting function used to implement weighting function 127 is determined by the specific signal processing operation to be performed. The second set of rays 143 traverse the second LCA 113 and are selectively attenuated, forming third set of rays 145. Third set of rays 145 are incident upon CCD 115, which converts rays 145 into corresponding electronic signals. These electronic signals are coupled to sampling circuitry 117 over signal input 133.

Sampling circuitry 117 samples the signals on signal input 133 at a rate determined by rate selection circuitry 121. The sampled signals are coupled to output buffer/amplifier circuitry 119 which produces an output signal representing processed data on output signal line 128.

According to one embodiment disclosed herein, the signals on input signal line 101 represent digitized video information. Although a halogen back light 107 is employed in the system of FIG. 1 for purposes of illustration, other stable light sources, such as a cold-cathode fluorescent lamp, may be used in place of the halogen back lamp. Although active-matrix liquid crystal arrays (LCAs) 109, 111, 113 are shown in the system of FIG. 1, other types of light valve devices may be employed as well. The system of FIG. 1 is equipped to perform signal processing operations such as real-time video compression and expansion. Such compression and expansion is performed irreversibly, but the temporal relationship of the original video signal is maintained.

Refer now to FIG. 2, which sets forth a hardware block diagram of a second embodiment of the optical signal processing system disclosed herein. An input signal representing a signal to be processed is coupled to signal input control 203 circuitry over input signal line 201. Signal input control 203 extracts DCT (discrete cosine transform) coefficients from the input signal and applies these DCT coefficients to a DCT driver circuit 205. The signal input control 203 circuitry also performs the function of coupling the input signal to a C/Q driver 207. C/Q driver 207 applies a weighting function to the input signal, as will be described in greater detail below.

A conventional tungsten lamp 211 provides illumination in the form of a first set of rays 212. The first set of rays 212 is incident upon a first liquid crystal array (LCA) 213 of an active-matrix, liquid crystal display (LCD) 218. The first LCA 213 is driven by DCT driver circuit 205. The DCT driver circuit 205 provides drive signals for the first LCA 213 , such that the light traversing the first LCA (and shown as second set of rays 214) represents the original optical image of the input signal converted to a DCT normalized value. In the present example, the signals provided by DCT driver 205 circuit are selected to be in the range of 0 to 255 to implement any of several image compression schemes well-known to those skilled in the art (JPEG, etc.). In this manner, the first LCA 213 applies a digitally-determined attenuation function to first set of rays 212, wherein the attenuation function specifies gray scale levels of 0 (black) through 255 (white) for each pixel of the LCA 213.

The resultant light output of first LCA 213, in the form of second set of rays 214, is then applied to a second LCA 215 of the active-matrix LCD 218. The second LCA 215 applies one or more weight basis functions to the second set of rays 214. The weight basis functions are generated from the C/Q driver 207 circuit acting on the second LCA 215. In the context of the present example which describes the processing of an audiovisual signal, the second LCA 215 operates as a light valve having a light output that represents a C/Q gray scale value within the compressed range of 0 (black) through 16 (white) for each pixel cell. The higher-frequency components of the video signal have values approaching white, and the lower-frequency components have values approaching black. The resultant light output of second LCA 215, in the form of third set of rays 216, represents the compressed signal (video and audio). Third set of rays 216 are converted to electrical signals by a conventional charge-coupled device (CCD) array 217.

According to a first embodiment of the system of FIG. 2, the output of CCD array 217 is processed by a video memory buffer 209, which may incorporate conventional video camera circuitry well-known to those

skilled in the art. The output of video memory buffer 209, representing a processed version of the input signal on input signal line 201, is placed on compressed output signal line 219. In the present example, this signal processing includes compression. The system of FIG. 2 is equipped to perform real-time compression of video and audio signals in no more than 90 percent of the time required by presently-existing video processing methods. In addition, the systems of FIGS. 1 and 2 may be used to implement virtually any type of existing compression technique, and these systems are transparent to the specific type of compression technique that is employed, i.e., JPEG, MPEG, etc.

According to a second embodiment of the system of FIG. 2, the output of CCD array 217 is processed by pixel match logic 222. Pixel match logic 222 may include conventional logic circuitry for comparing the values of pixels. Pixel match logic 222 is employed in operational environments where it is desired to perform motion estimation procedures. If pixel match logic 222 locates a pixel match, signifying, for example, that a pixel in a given position within a frame has not changed in value from a given frame to the immediately succeeding frame, then pixel match logic 222 produces an output signal which specifies the frame number and the block number of the matching pixel on motion estimation output signal line 225. If pixel match logic 222 finds no pixel match, then pixel match logic 222 passes the CCD array 217 output to video memory buffer 209. The output of video memory buffer 209 is a compressed output signal on compressed output signal line 219.

Refer now to FIG. 3 which sets forth the contents of representative images at various signal processing steps in the system of FIG. 2. Image 308 represents the original image at input signal line 201 (FIG. 2). The image is organized into a 4 x 4 array of pixels, including pixel 303 having a value of I_1, and pixel 304 having a value of I_{16}. Pixels relatively close to pixel 304 represent relatively low-frequency components of the original image, and pixels relatively close to pixel 303 represent relatively high-frequency components of the original image.

Image 308 is processed by first LCA 213 (FIG. 2) to produce image 310 (FIG. 3) which is represented by second set of rays 214 (FIG. 2). Pixel 305 (FIG. 3) has a value C_1 of 255, and pixel 307 has a value C_{16} of 0. Each pixel 305, 307 of image 310 is produced by a corresponding pixel of the first LCA 213 (FIG. 2) acting upon the incident illumination from the tungsten lamp 211 (FIG. 2). Each pixel of first LCA 213 (FIG. 2), and each corresponding pixel of image 310 (FIG. 3) represents a specific frequency component of the original image. The amplitude value of each pixel (i.e., 255 in the case of pixel 305, FIG. 3, and 0 in the case of pixel 307) represents the magnitude value of each frequency component. In the present example, these magnitude values are selected to be in the range of 0 - 255.

The frequency components of each pixel 305, 307 in image 310 (FIG. 3), as represented by corresponding pixels of first LCA 213 (FIG. 2) and second set of rays 214, are now divided by corresponding entries in a Q table. The Q table is stored in C/Q driver 207 (FIG. 2), which applies the Q table to image 310 (FIG. 3). The Q table may be hardwired into C/Q driver 207 (FIG. 2), or the Q table may be placed into random-access memory (RAM) or read-only memory (ROM) associated with C/Q driver 207. The C/Q driver 207 controls each pixel of second LCA 215 to selectively attenuate second set of rays 214. Since second set of rays 214 includes representations of each pixel 305, 307 of image 310 (FIG. 3), this selective attenuation is performed such that each pixel 305, 307 is divided by a corresponding entry of the Q table of C/Q driver 207 (FIG. 2). The resultant light output from second LCA 215, in the form of third set of rays 216, represents quantized DCT coefficients corresponding to the original image.

The third set of rays 216 (FIG. 2) includes a representation of image 312 (FIG. 3). Image 312 is applied to CCD array 217 (FIG. 2) which consists of an array of charge-coupled device cells. The video memory buffer 209 electronically scans the CCD array 217 in a conventional zigzag pattern. This pattern is shown in FIG. 3 as scanning lines a-a' b-b', c-c', d-d', e-e', and f-f'. The zigzag pattern is employed to organize the frequency components of the processed audio/video signal, such that the frequency components of the output signal are presented in ascending frequency order.

FIG. 4 is a combined hardware and data structure diagram setting forth a third embodiment of the signal processing system disclosed herein for implementing JPEG video compression. An audio/video input signal to be JPEG-compressed is fed to data input line 401. The audio/visual input signal includes a digital representation of image 303 (FIG. 3). Various well-known methods exist for converting conventional analog audio/video signals into the format of image 303. Image 303 is in the form of a 4 x 4 pixel array, and an illustrative example of the contents of this array are set forth in FIG. 4 as first array 409. An offset 405 generator coupled to a subtractor 403 applies an offset function to first array 409. A DCT 407 function is then applied to the offset array, yielding second array 411. Note that this second array 411 is represented in FIG. 2 by second set of rays 214. DCT 407 (FIG. 4) may be implemented, for example, by DCT driver 205 and first LCA 213 (FIG. 2).

Returning now to FIG. 4, a zigzag run encoder 413 in parallel with a difference encoder 417 are applied to the second array 411, followed by a Q 421 function. The parallel combination of zigzag run encoder 413 and difference encoder 417, followed by Q 421 function, may be implemented by the C/Q driver 207 and the second LCA 215 (FIG. 2). After the second array 411 has been processed by the parallel combination of zigzag run encoder 413 and difference encoder 417, but prior to the application of the Q 421 function, the second array 411 is transformed into third array 429. After application of

Q function 421, the third array 429 is transformed into a fourth array 431. The Q function 421 is implemented using a Q table 419 which, in the present example, is a 4 x 4 array wherein each element of the array has a value of 10. Therefore, the Q function 421 effectively performs a division operation (divide by ten) on the third array 429, rounding off the result to the nearest integer.

The data contained in fourth array 431 are compressed using a VLC (variable length coder) 423, which applies a Huffman table function to the fourth array 431. Note that the array entries of the first, second, third and fourth arrays 409, 411, 429, 431, respectively, are in conventional decimal (base ten) notation. The Huffman table associates each of a plurality of decimal (base ten) integers with corresponding binary codes. An illustrative example of a Huffman table is shown in FIG. 4, where the first column heading entitled "symbols" refers to decimal (base ten) integers, and the second column headed "code" refers to the binary code that is assigned to each symbol. For example, the table specifies that the symbol +2 corresponds to a binary code of 110. VLC 427 replaces each symbol (i.e., each entry) in the fourth array 431 with the corresponding code from the Huffman table, thereby generating fifth array 425.

An inverse VLC 427 transform is applied to the fifth array 425 to generate sixth array 435, and an inverse Q 437 transform is applied to the sixth array 435 to generate a seventh array 433. The inverse Q 437 transform is determined by the contents of Q table 439. The output of inverse Q 437 transform is processed by the parallel combination of a zigzag run decoder 443 and a difference decoder 441 to generate eighth array 447. Note that third, fourth, fifth, sixth, and seventh arrays 429, 431, 425, 435, 433, respectively, are one-dimensional arrays, whereas eighth array 447 is a 4 x 4 array having the same dimensions as first and second arrays 409, 411. Eighth array 447 is subjected to an inverse DCT 445 transform, and a fixed offset is added to the array by an offset 453 generator and a summer 451, to generate ninth array 449. The ninth array 449 represents decoded data output 455 compressed in the JPEG format. The data compression performed by the system of FIG. 4 is a "lossy" compression in the sense that the compression is irreversible.

Claims

1. A signal processing system for processing an input signal in real time CHARACTERIZED BY:

   (a) light valve array means for selectively attenuating light incident thereupon in response to electronic control signals;
   (b) light source means for providing illumination;
   (c) light-sensitive array means for producing electronic output signals in response to light incident thereupon, the electronic output signals representing a processed version of the input signal; and
   (d) control means for generating and applying electronic control signals to the light valve array in response to the input signal, wherein the electronic control signals are generated from the input signal and are adapted for implementing an arbitrarily-selected signal processing operation;
   the light valve array means situated between the light source means and the light-sensitive array means, such that the light source means is selectively attenuated by the light valve array means, and such that the selectively attenuated light is incident upon the light-sensitive array means.

2. A signal processing system for processing an input signal in real time CHARACTERIZED BY:

   (a) first light valve array means for selectively attenuating light incident thereupon in response to the input signal;
   (b) second light valve array means for selectively attenuating light incident thereupon in response to electronic control signals;
   (c) light source means for providing illumination;
   (d) light-sensitive array means for producing electronic output signals in response to light incident thereupon, the electronic output signals representing a processed version of the input signal; and
   (e) control means for generating and applying electronic control signals to the light valve array, wherein the electronic control signals are adapted for implementing an arbitrarily-selected signal processing operation;
   the light valve array means situated between the light source means and the light-sensitive array means, such that the light source means is selectively attenuated by the light valve array means, and such that the selectively attenuated light is incident upon the light-sensitive array means.

3. A signal processing system as set forth in claim 1 or 2, wherein the first or first mentioned light valve array means comprises a liquid crystal array having a plurality of light valve pixel elements arranged into an array, each light valve pixel element defining a light valve providing for the selective attenuation of light incident thereupon in response to the electronic control signals. or input signals.

4. A signal processing system as set forth in claim 1, 2, or 3, further comprising sampling means, coupled

to the light-sensitive array means, for sampling the light-sensitive array means at a predetermined sampling rate.

5. A signal processing system as set forth in claim 4, further comprising rate control means, coupled to the sampling means, for adjusting the predetermined sampling rate.

6. A signal processing system as set forth in claim 5, further comprising output buffer means, coupled to the sampling means, for buffering the output of the sampling means to produce a buffered output signal.

7. A signal processing system as set forth in claim 6, wherein the output buffer means is coupled to the control means, and wherein the electronic control signals are a function of the buffered output signal and the input signal.

8. A signal processing system as set forth in claim 2 or 3, wherein the control means further comprises DCT coefficient extraction means for calculating DCT coefficients from the input signal.

9. A signal processing system as set forth in claim 8, wherein the control means further comprises quantization coefficient extraction means for calculating quantization coefficients from the input signal.

10. A signal processing system as set forth in claim 3, wherein the light-sensitive array means comprises a charge-coupled device (CCD).

11. A signal processing system as set forth in claim 10, wherein the light source means comprises a halogen back light.

12. A signal processing system as set forth in claim 9, wherein the control means further comprises memory means for storing a table of quantization coefficients and a weighting function.

13. A signal processing system as set forth in claim 12, wherein the control means further comprises processor means coupled to the rate selection means and the memory means for selecting a predetermined sampling rate based upon the contents of the memory means.

14. A signal processing system as set forth in claim 2, wherein the second light valve array means comprises a liquid crystal array having a plurality of light valve pixel elements arranged into an array, each light valve pixel element defining a light valve providing for the selective attenuation of light incident thereupon in response to the electronic control signals.

15. A signal processing system as set forth in claim 3, wherein the input signal represents digitized video information, the light source means is a cold-cathode fluorescent or halogen lamp, and the light-sensitive array means is an area-array charge-coupled device (CCD).

16. A signal processing system as set forth in claim 3, wherein the input signal represents digitized video information, the light source means is a cold-cathode fluorescent or halogen lamp, and the light-sensitive array means is an area-array charge-coupled device (CCD).

17. A signal processing system as set forth in claim 4, wherein the input signal represents digitized video information, the light source means is a cold-cathode fluorescent or halogen lamp, and the light-sensitive array means is an area-array charge-coupled device (CCD).

18. A signal processing system as set forth in claim 1, wherein the arbitrarily-selected signal processing operation includes real-time video compression.

19. A signal processing system as set forth in claim 18, wherein the arbitrarily-selected signal processing operation includes real-time JPEG video compression and expansion.

20. A signal processing system as set forth in claim 3, wherein the arbitrarily-selected signal processing operation includes real-time video compression.

21. A signal processing system as set forth in claim 20, wherein the arbitrarily-selected signal processing operation includes real-time JPEG video compression and expansion.

22. A signal processing system as set forth in claim 20, wherein the signal processing operation includes motion compensation for video coding.

FIG. 1

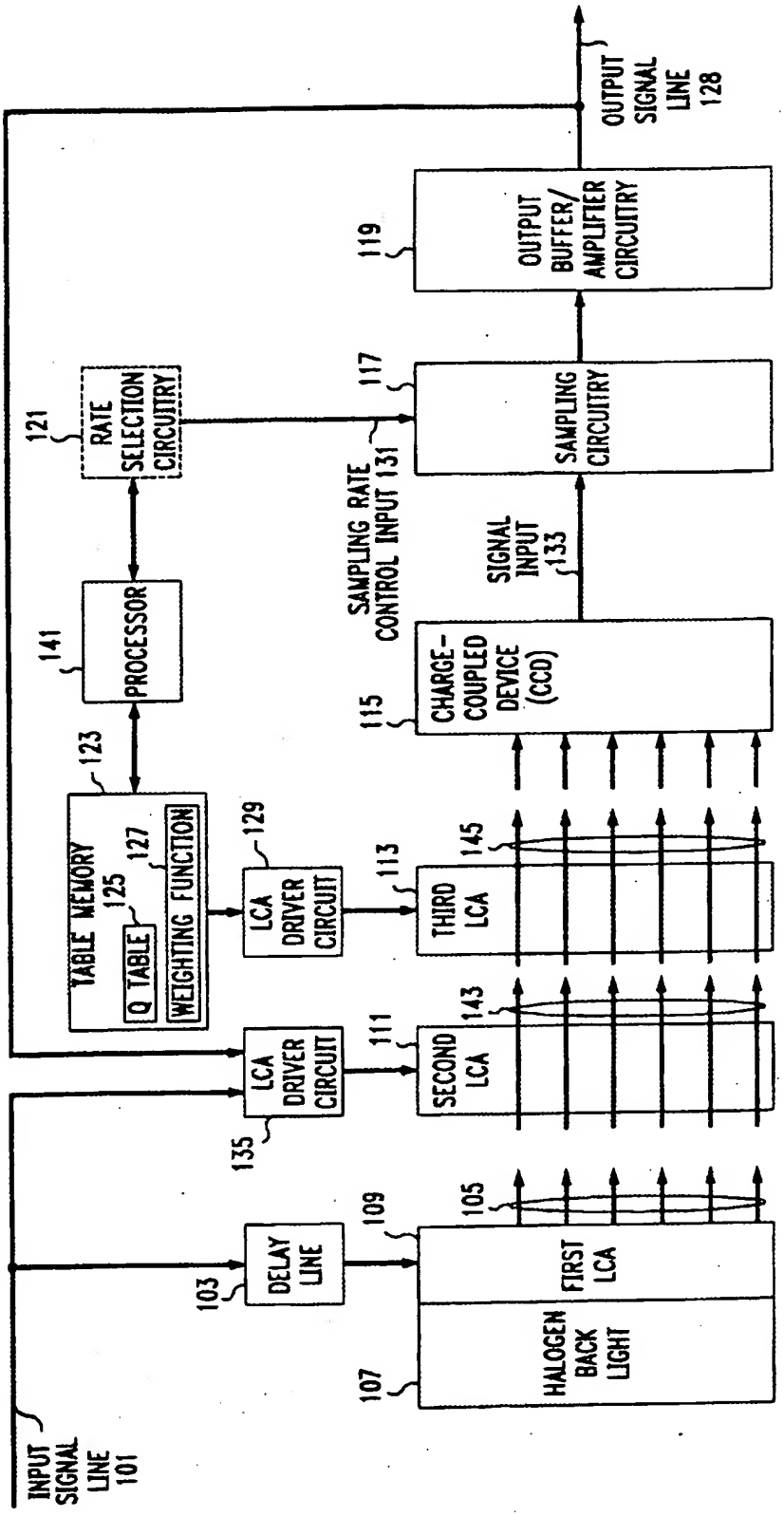

INPUT SIGNAL LINE 101
DELAY LINE
103
109
HALOGEN BACK LIGHT
107
FIRST LCA
105
LCA DRIVER CIRCUIT
135
111
SECOND LCA
143
LCA DRIVER CIRCUIT
129
113
THIRD LCA
145
TABLE MEMORY
125
Q TABLE
127
WEIGHTING FUNCTION
123
PROCESSOR
141
RATE SELECTION CIRCUITRY
121
CHARGE-COUPLED DEVICE (CCD)
115
SIGNAL INPUT
133
SAMPLING RATE CONTROL INPUT 131
SAMPLING CIRCUITRY
117
OUTPUT BUFFER/ AMPLIFIER CIRCUITRY
119
OUTPUT SIGNAL LINE 128

FIG. 2

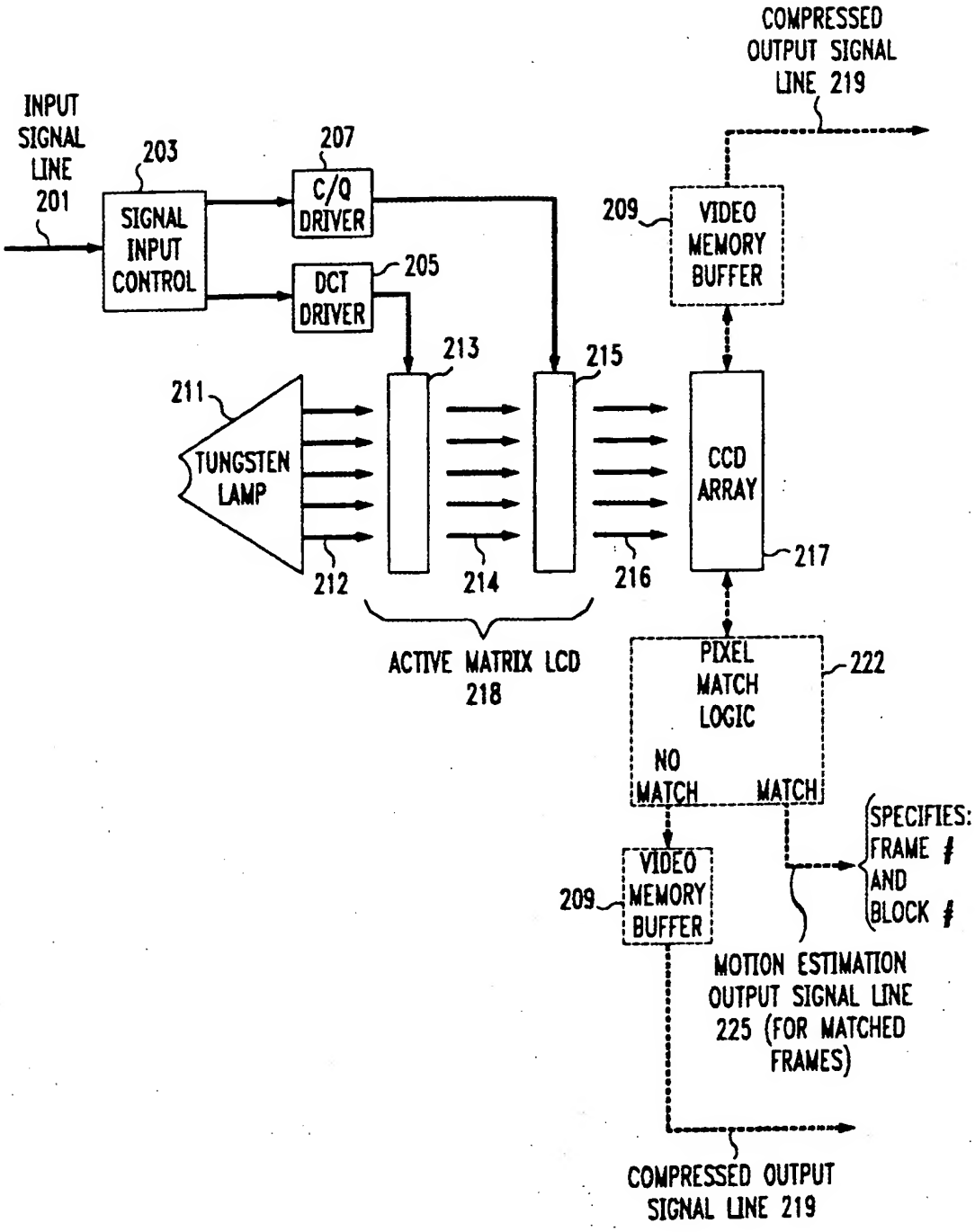
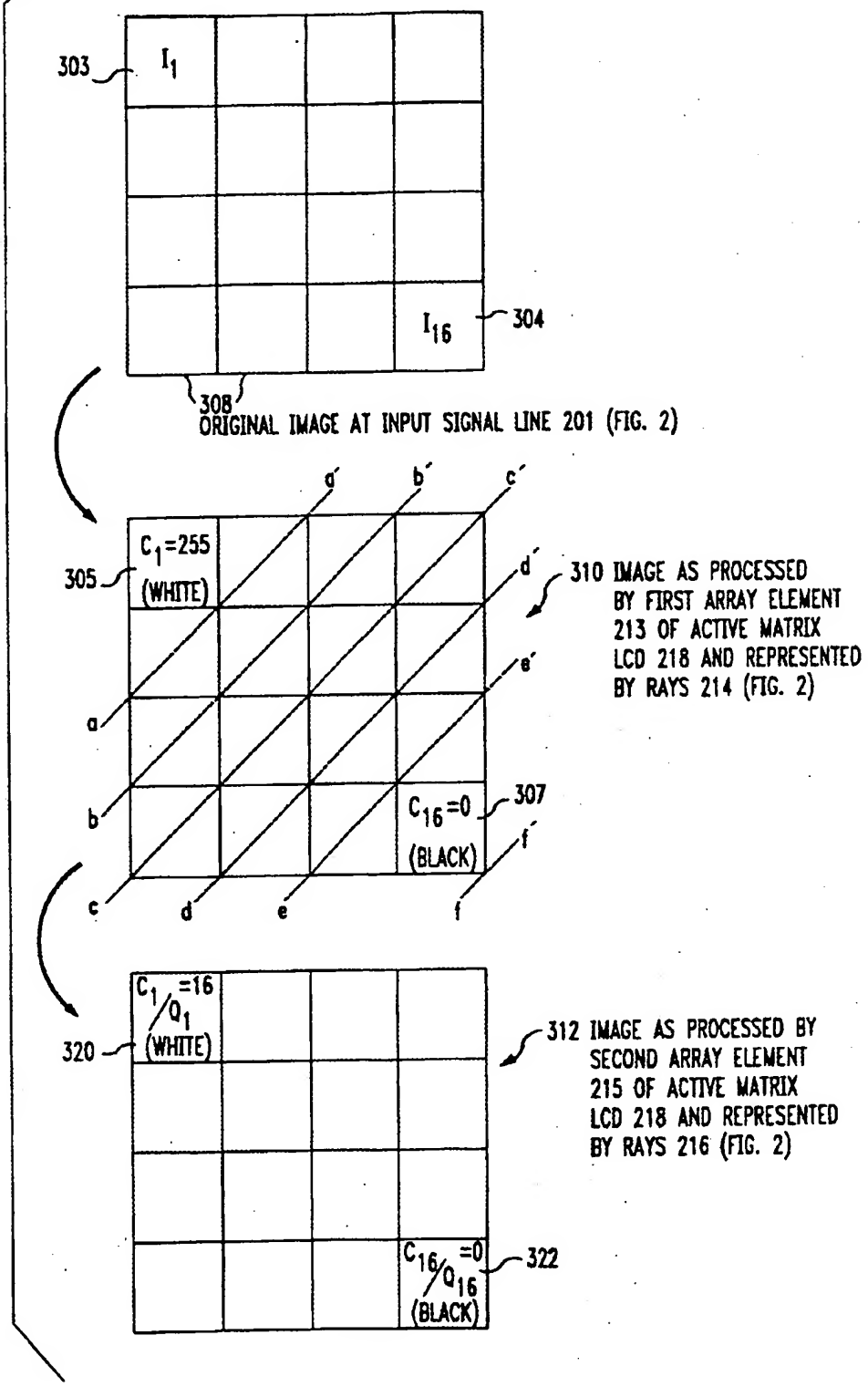

COMPRESSED OUTPUT SIGNAL LINE 219
INPUT SIGNAL LINE 201
203
SIGNAL INPUT CONTROL
207
C/Q DRIVER
205
DCT DRIVER
209
VIDEO MEMORY BUFFER
211
TUNGSTEN LAMP
213
215
CCD ARRAY
217
212
214
216
ACTIVE MATRIX LCD 218
PIXEL MATCH LOGIC
222
NO MATCH
MATCH
SPECIFIES: FRAME # AND BLOCK #
209
VIDEO MEMORY BUFFER
MOTION ESTIMATION OUTPUT SIGNAL LINE 225 (FOR MATCHED FRAMES)
COMPRESSED OUTPUT SIGNAL LINE 219

FIG. 3


303
I_1
I_{16}
304
308
ORIGINAL IMAGE AT INPUT SIGNAL LINE 201 (FIG. 2)
a'
b'
c'
d'
e'
f'
C_1=255
(WHITE)
305
310 IMAGE AS PROCESSED BY FIRST ARRAY ELEMENT 213 OF ACTIVE MATRIX LCD 218 AND REPRESENTED BY RAYS 214 (FIG. 2)
a
b
c
d
e
f
C_{16}=0
(BLACK)
307
C_1/Q_1=16
(WHITE)
320
312 IMAGE AS PROCESSED BY SECOND ARRAY ELEMENT 215 OF ACTIVE MATRIX LCD 218 AND REPRESENTED BY RAYS 216 (FIG. 2)
C_{16}/Q_{16}=0
(BLACK)
322

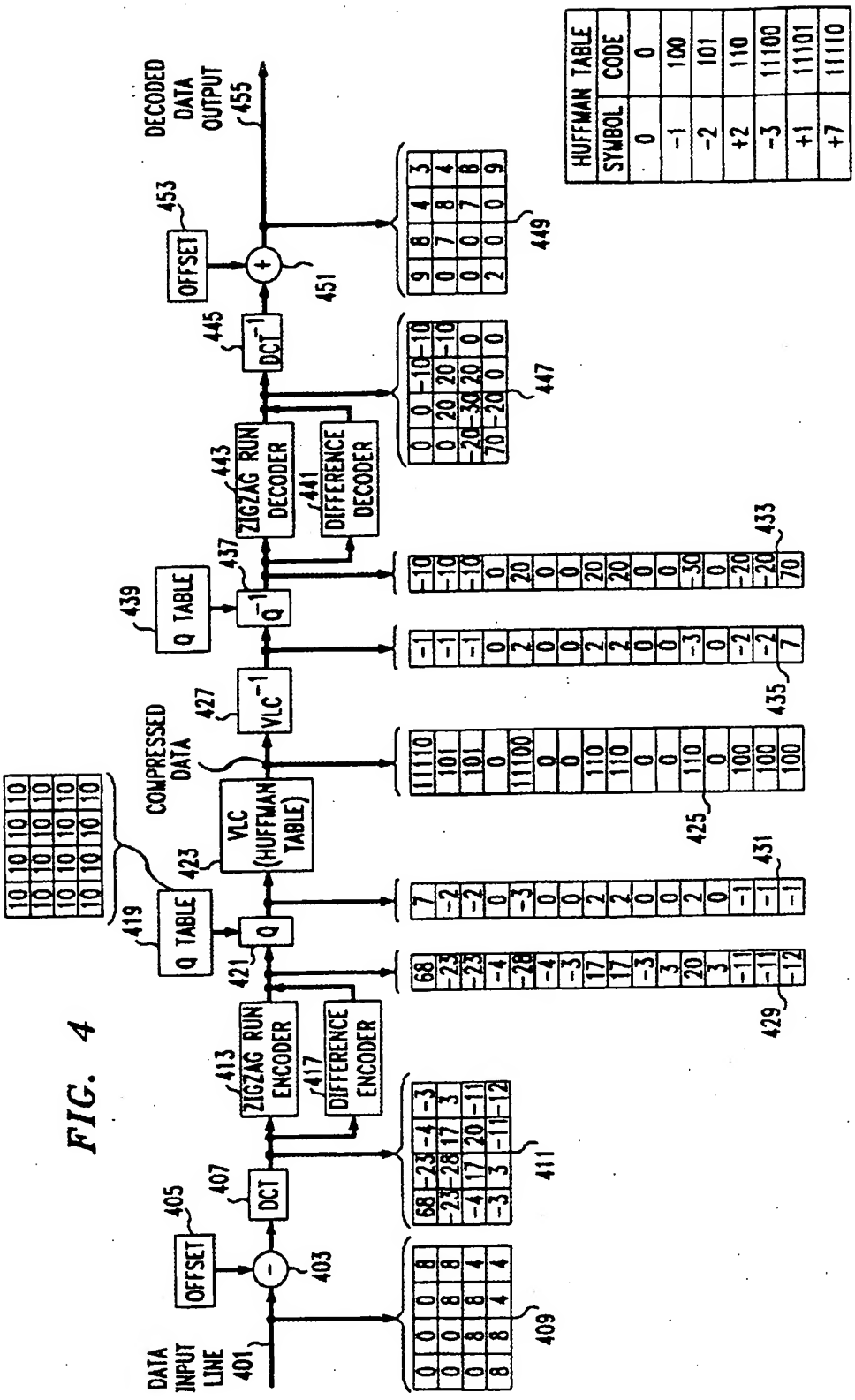

DATA INPUT LINE
401
OFFSET
405
403
DCT
407
ZIGZAG RUN ENCODER
413
DIFFERENCE ENCODER
417
Q TABLE
419
Q
421
VLC (HUFFMAN TABLE)
423
COMPRESSED DATA
VLC⁻¹
427
Q TABLE
439
Q⁻¹
437
ZIGZAG RUN DECODER
443
DIFFERENCE DECODER
441
DCT⁻¹
445
OFFSET
453
DECODED DATA OUTPUT
455
451
HUFFMAN TABLE
SYMBOL
CODE
0
0
-1
100
-2
101
+2
110
-3
11100
+1
11101
+7
11110

FIG. 4